7

(19)日本国特許庁(JP)

# (12) 公開実用新案公報(U)

(11) 実用新案出願公開番号

# 実開平6-23276

(43)公開日 平成6年(1994)3月25日

(51)Int.Cl.<sup>5</sup>

職別記号

FI

技術表示箇所

H 0 5 K 1/18

1/18 7/12 D 9154-4E

庁内整理番号

M 7301-4E

審査請求 未請求 請求項の数2(全 2 頁)

(21)出願番号

実願平4-60665

(71)出願人 000003078

株式会社東芝

(22)出願日

平成 4年(1992) 8月28日

神奈川県川崎市幸区堀川町72番地

(72)考案者 髙見 昌之

神奈川県川崎市幸区小向東芝町 1 番地 株

式会社東芝小向工場内

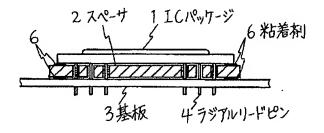
(74)代理人 弁理士 則近 憲佑

### (54) 【考案の名称】 I Cパッケージの取付構造

## (57)【要約】

【目的】 動作不良や絶縁不良が起こりにくく、良好な特性が得られる I Cパッケージの取付構造を提供することを目的とする。

【構成】 基板3に貫通されて導通をとるべく複数のライアルリードピン4を備えてなるICパッケージ1と前記基板3との間に絶縁性で弾性体のスペーサ2を介在したこと特徴とする。



\*10

## 【実用新案登録請求の範囲】

【請求項1】 基板に貫通されて導通をとるべく複数の電極ピンを備えてなるICパッケージと、前記ICパッケージと前記基板との間に露出した前記複数の電極ピンを隠蔽するように前記ICパッケージと前記基板との間に絶縁物を介在したことを特徴とするICパッケージの取付構造。

1

【請求項2】 前記絶縁物は粘着性を有することを特徴とする請求項1記載のICパッケージの取付構造。

【図面の簡単な説明】

\*【図1】本考案の一実施例の構成を示す図。

【図2】図1の断面を示す図。

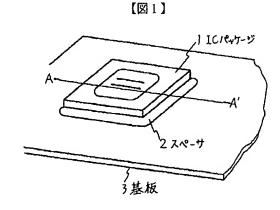
【図3】スペーサの一例を示す斜視図

【図4】図3と異なるスペーサの一例を示す斜視図。

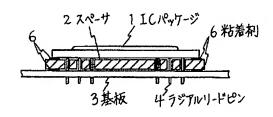
【図5】従来の I Cパッケージの取り付け構造を示す断面図。

### 【符号の説明】

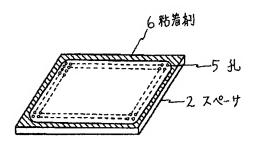
1…ICパッケージ, 2…スペーサ, 3…基板, 4…ラジアルリードピン, 5…孔, 6…粘着剤



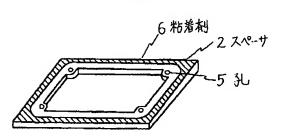
【図2】



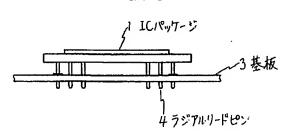
[図3]



[図4]



[図5]



# 【考案の詳細な説明】

[0001]

# 【産業上の利用分野】

本考案は、電子回路を実装してなるプリント基板へのICパッケージの取付構造に関する。

[0002]

## 【従来の技術】

近年、半導体プロセス技術の進展によりICの大規模化が進み、中でもゲートアレイはその汎用性の高さ、開発期間の短さから各種分野で盛んに用いられている。

この大規模のゲートアレイは、入出力信号及び電源グランド等の接続のため多数の電極を備え、数百本の入出力ピンを備えることもめずらしくない。

## [0003]

このパッケージの代表的なものにPGA(ピングリッドアレイ)がある。このパッケージは、通常はセラミック等の本体のいずれか片方の面に格子状にラジアルリードピンが取り付けられて構成される。プリント基板に実装するときはあらかじめPGAのリードピンと合致するように孔を設けておき、ピンを挿入した後に半田付けする。

### [0004]

図5に上述した従来のICパッケージの取付構造の断面図を示す。プリント基板3にICパッケージ1を取り付る際に注意すべきことは、ラジアルリードピン4をその根元まで挿入しないで必ずICパッケージ1と基板3との間に空隙を設ける必要がある点である。この空隙の存在により、基板3に加わる外力がリードピン4のICパッケージ1側の根元に直接加わらない。

## [0005]

しかしながら、このような取り付けを行ってある機器内にこの基板を収容して使用する場合、とくに強制空冷で使用したりすると、この I C パッケージ 1 と基板 3 間の空隙にホコリが蓄積しやすい。したがって、外部環境が劣悪の場合はピン間の絶縁不良が発生する恐れがあった。

# [0006]

また、試験、修理などの作業中、この空隙内部に金属ゴミ等をいれてしまうと 取り除くのが大変であるばかりでなく動作不良をおこしかねないという問題があった。

# [0007]

# 【考案が解決しようとする課題】

上述したように、従来のICパッケージ取付構造では、ICパッケージと基板 との間に生じた空隙が原因で動作不良や絶縁不良が発生するという問題点があっ た。

## [0008]

本考案は上記事情を考慮してなされたもので、多極のラジアルリードピンを備えたICパッケージを基板に取付ける際、上記した空隙を生じないようにして、動作不良や絶縁不良が起こりにくく良好な特性が得られるICパッケージの取付構造を提供することを目的とする。

# [0009]

# 【課題を解決するための手段】

上記課題を解決するために本考案は、基板に貫通されて導通をとるべく複数の電極ピンを備えてなるICパッケージと、前記ICパッケージと前記基板との間に露出した前記複数の電極ピンを隠蔽するように前記ICパッケージと前記基板との間に絶縁物を介在したこと特徴とする。

## [0010]

# 【作用】

上記した構成において、ICパッケージと基板との間に介在された絶縁物が前記ICパッケージと前記基板との間の空隙を埋めてICパッケージと基板との間の複数の電極ピンを外部から隠蔽するとともに、基板に加わる外力を吸収してこの外力がリードピンのICパッケージ側の根元に直接加わるのを防ぐ。

# [0011]

## 【実施例】

以下、本考案の実施例を図面を参照して説明する。

図1は本考案の一実施例であるICパッケージの取付構造、図2は図1中のA-A で切った断面図を示す。図1、図2において、図5と同一部分には同一符号を付し、詳しい説明は省略する。

# [0012]

図1及び図2において、2は絶縁性のスペーサである。このスペーサ2は、ICパッケージ1を基板3に取り付ける際に、あらかじめ基板3に取り付けられる。そして、図2から明らかなように、このスペーサ2はICパッケージ1と基板3の間のラジアルリードピン4が露出しないようになっている。

# [0013]

スペーサ2はその外周部に粘着剤6が塗布されている。この粘着剤6はICパッケージ1が浮いてスペーサ2との間に空隙ができてしまうことのないように設けれているもので、接着剤でもかまわない。

## [0014]

また、スペーサ2の材料としてはシリコンゴム等の耐熱性のある弾性体であれば何でもよい。さらにスペーサ2は均一な厚みを備え、図3に示すようにラジアルリードピンが貫通する孔5が形成されている。

### [0015]

このスペーサ2は上記した構成に限ることはない。たとえば図4に示すように 位置決め用の孔5を四隅に配して他の部分はくり抜いても図1や図3に示したスペーサ2と同様の作用が得られる。さらに、図示しないが、孔5を設けず外周部 のみにスペーサを介するようにしても良いことは言うまでもない。

### [0016]

以上述べたように、本考案によれば、ICパッケージと基板との間の空間にゴミなどが侵入しないので、動作不良や絶縁不良などを起こすことはない。さらに、取り付け作業中の事故も防ぐことができる。また、一般に、PGA型のICにおいてはチップの放熱のためにフィンが上面に取り付けられるが、本考案の構造を用いれば、通風断面積が少なくてすむ。すなわち、IC下部の空気の流れを止めることにより、強制空冷の効果をより大きくすることができる。

さらに、スペーサそのものは弾性体であり、基板にかかるストレス(外力)に

対してラジアルリードピンの根元が弱くなることはない。

[0017]

# 【考案の効果】

以上詳述したように、本考案によればICパッケージと基板の間に空隙がないので動作不良や絶縁不良は発生しなくなり良好な特性を得ることができる。

JPO and INPIT are not responsible for any damages caused by the use of this translation.

- 1. This document has been translated by computer. So the translation may not reflect the original precisely.
- 2.\*\*\*\* shows the word which can not be translated.
- 3.In the drawings, any words are not translated.

## **CLAIMS**

[The scope of a claim for utility model registration]

[Claim 1] Mounting structure of an IC package intervening an insulating material between said IC package and said substrate so that said two or more electrode pins exposed between an IC package provided with two or more electrode pins in order to penetrate to a substrate and to take a flow, and said IC package and said substrate may be concealed.

[Claim 2] Mounting structure of the IC package according to claim 1, wherein said insulating material has adhesiveness.

JPO and INPIT are not responsible for any damages caused by the use of this translation.

1. This document has been translated by computer. So the translation may not reflect the original precisely.

2.\*\*\*\* shows the word which can not be translated.

3.In the drawings, any words are not translated.

### **DETAILED DESCRIPTION**

[Detailed explanation of the device]

[0001]

[Industrial Application]

This design is related with the mounting structure of the IC package to the printed circuit board which mounts an electronic circuit.

[0002]

[Description of the Prior Art]

In recent years, large-scale-ization of IC progresses by progress of semiconductor process technique, and the gate array is especially used briskly [various fields] from the height of the flexibility, and the shortness of the development cycle.

As for this large-scale gate array, it is not new to have many electrodes for connection of an input output signal, a power supply ground, etc., and to have hundreds of output pins, either. [0003]

PGA (pin grid array) is one of the typical things of this package. A radial lead pin is usually attached to any of main parts, such as ceramics, or field of one of the two in the shape of a lattice, and this package is constituted. The hole is provided so that it may agree with the lead pin of PGA beforehand, when mounted in a printed circuit board, and it solders, after inserting a pin.

[0004]

The sectional view of the mounting structure of the conventional IC package mentioned above to drawing 5 is shown. What IC package 1 should be taken to the printed circuit board 3, and it should be careful of in the \*\*\*\* case is the point that it is necessary to certainly provide an opening between IC package 1 and the substrate 3 without inserting the radial lead pin 4 to the root. By existence of this opening, the external force added to the substrate 3 is not directly added to the root by the side of IC package 1 of the lead pin 4.

[0005]

However, if it is used especially by an air cooling with blower when using it, accommodating this substrate in the apparatus which has performed such attachment, it will be easy to accumulate dust in the opening between this IC package 1 and the substrate 3. Therefore, when outside environment was inferior, there was a possibility that the bad insulation between pins might occur.

[0006]

There was a problem that it is not only serious to remove if metallic dust etc. are put during the work of an examination, repair, etc. and into the inside of this opening, but it might raise a malfunction.

[0007]

[Problem(s) to be Solved by the Device]

As mentioned above, in the conventional IC package mounting structure, there was a problem that a malfunction and bad insulation occurred owing to the opening produced between the IC package and the substrate.

[8000]

As this design was made in consideration of the above-mentioned situation and does not produce the opening described above when attaching the IC package provided with the multipolar radial lead pin to a substrate, it aims at providing the mounting structure of the IC package from which the good characteristic is obtained that neither a malfunction nor bad insulation can happen easily.

[0009]

[Means for Solving the Problem]

An IC package provided with two or more electrode pins in order to solve an aforementioned problem, to penetrate this design to a substrate and to take a flow, It is considered as the intervening-between said IC package and said substrate-insulating material feature so that said two or more electrode pins exposed between said IC package and said substrate might be concealed.

[0010]

[Function]

While the insulating material which intervened between the IC package and the substrate fills the opening between said IC package and said substrate and conceals two or more electrode pins between an IC package and a substrate from the outside in the above-mentioned composition, It prevents absorbing the external force added to a substrate and adding this external force to the root by the side of the IC package of a lead pin directly.

[0011]

[Example]

Hereafter, the example of this design is described with reference to drawings.

The mounting structure of the IC package whose <u>drawing 1</u> is one example of this design, and <u>drawing 2</u> show the sectional view cut with A-A' in <u>drawing 1</u>. In <u>drawing 1</u> and <u>drawing 2</u>, identical codes are given to <u>drawing 5</u> and identical parts, and detailed explanation is omitted. [0012]

In <u>drawing 1</u> and <u>drawing 2</u>, 2 is an insulating spacer. When this spacer 2 attaches IC package 1 to the substrate 3, it is beforehand attached to the substrate 3. And the radial lead pin 4 between IC package 1 and the substrate 3 exposes this spacer 2 so that clearly from <u>drawing 2</u>. [0013]

As for the spacer 2, the binder 6 is applied to the peripheral part. This binder 6 can be formed so that IC package 1 may float and an opening may not be made between the spacers 2, and adhesives may be sufficient as it.

[0014]

It is [anything] good if it is an existing elastic body of heat resistance, such as silicone rubber, as a material of the spacer 2. Furthermore, the spacer 2 is provided with uniform thickness and the hole 5 which a radial lead pin penetrates as shown in <u>drawing 3</u> is formed.

[0015]

This spacer 2 is not restricted to the above-mentioned composition. For example, the same operation as the spacer 2 which allotted the hole 5 for positioning to four corners, and showed drawing 1 and drawing 3 other partial foil \*\*\*\*\*\*\*\* as shown in drawing 4 is obtained. Although not illustrated, it cannot be overemphasized that the hole 5 is not formed but it may be made to pass a spacer only to a peripheral part.

[0016]

As stated above, since garbage etc. do not trespass upon the space between an IC package and a substrate according to this design, neither a malfunction nor bad insulation is woken up. The accident under attachment work can also be prevented. Generally, although a fin is attached to the upper surface in IC of PGA for heat dissipation of a chip, if the structure of this design is used, there will be few ventilation cross—section areas and they will end. That is, the effect of an air cooling with blower can be enlarged more by stopping the flow of the air of IC lower part. The spacer itself is an elastic body and the root of a radial lead pin does not become weak to the stress (external force) concerning a substrate.

[0017]

[Effect of the Device]

Since there is no opening between an IC package and a substrate according to t	
explained in full detail above, it stops occurring and a malfunction and the bad in	sulation can get
the good characteristic.	

JPO and INPIT are not responsible for any damages caused by the use of this translation.

- 1. This document has been translated by computer. So the translation may not reflect the original precisely.
- 2.\*\*\* shows the word which can not be translated.
- 3.In the drawings, any words are not translated.

## **TECHNICAL FIELD**

[Industrial Application]

This design is related with the mounting structure of the IC package to the printed circuit board which mounts an electronic circuit.

[0002]

JPO and INPIT are not responsible for any damages caused by the use of this translation.

- 1. This document has been translated by computer. So the translation may not reflect the original precisely.
- 2.\*\*\*\* shows the word which can not be translated.
- 3.In the drawings, any words are not translated.

### **PRIOR ART**

[Description of the Prior Art]

In recent years, large-scale-ization of IC progresses by progress of semiconductor process technique, and the gate array is especially used briskly [various fields] from the height of the flexibility, and the shortness of the development cycle.

As for this large-scale gate array, it is not new to have many electrodes for connection of an input output signal, a power supply ground, etc., and to have hundreds of output pins, either. [0003]

PGA (pin grid array) is one of the typical things of this package. A radial lead pin is usually attached to any of main parts, such as ceramics, or field of one of the two in the shape of a lattice, and this package is constituted. The hole is provided so that it may agree with the lead pin of PGA beforehand, when mounted in a printed circuit board, and it solders, after inserting a pin.

[0004]

The sectional view of the mounting structure of the conventional IC package mentioned above to drawing 5 is shown. What IC package 1 should be taken to the printed circuit board 3, and it should be careful of in the \*\*\*\* case is the point that it is necessary to certainly provide an opening between IC package 1 and the substrate 3 without inserting the radial lead pin 4 to the root. By existence of this opening, the external force added to the substrate 3 is not directly added to the root by the side of IC package 1 of the lead pin 4. [0005]

However, if it is used especially by an air cooling with blower when using it, accommodating this substrate in the apparatus which has performed such attachment, it will be easy to accumulate dust in the opening between this IC package 1 and the substrate 3. Therefore, when outside environment was inferior, there was a possibility that the bad insulation between pins might occur.

[0006]

There was a problem that it is not only serious to remove if metallic dust etc. are put during the work of an examination, repair, etc. and into the inside of this opening, but it might raise a malfunction.

[0007]

JPO and INPIT are not responsible for any damages caused by the use of this translation.

- 1. This document has been translated by computer. So the translation may not reflect the original precisely.
- 2.\*\*\*\* shows the word which can not be translated.
- 3.In the drawings, any words are not translated.

## **EFFECT OF THE INVENTION**

[Effect of the Device]

Since there is no opening between an IC package and a substrate according to this design as explained in full detail above, it stops occurring and a malfunction and the bad insulation can get the good characteristic.

JPO and INPIT are not responsible for any damages caused by the use of this translation.

- 1. This document has been translated by computer. So the translation may not reflect the original precisely.
- 2.\*\*\*\* shows the word which can not be translated.
- 3.In the drawings, any words are not translated.

#### TECHNICAL PROBLEM

[Problem(s) to be Solved by the Device]

As mentioned above, in the conventional IC package mounting structure, there was a problem that a malfunction and bad insulation occurred owing to the opening produced between the IC package and the substrate.

[8000]

As this design was made in consideration of the above-mentioned situation and does not produce the opening described above when attaching the IC package provided with the multipolar radial lead pin to a substrate, it aims at providing the mounting structure of the IC package from which the good characteristic is obtained that neither a malfunction nor bad insulation can happen easily.

[0009]

JPO and INPIT are not responsible for any damages caused by the use of this translation.

- 1. This document has been translated by computer. So the translation may not reflect the original precisely.
- 2.\*\*\*\* shows the word which can not be translated.
- 3.In the drawings, any words are not translated.

### **MEANS**

[Means for Solving the Problem]

An IC package provided with two or more electrode pins in order to solve an aforementioned problem, to penetrate this design to a substrate and to take a flow, It is considered as the intervening-between said IC package and said substrate-insulating material feature so that said two or more electrode pins exposed between said IC package and said substrate might be concealed.

[0010]

JPO and INPIT are not responsible for any damages caused by the use of this translation.

- 1. This document has been translated by computer. So the translation may not reflect the original precisely.
- 2.\*\*\*\* shows the word which can not be translated.
- 3.In the drawings, any words are not translated.

### OPERATION

## [Function]

While the insulating material which intervened between the IC package and the substrate fills the opening between said IC package and said substrate and conceals two or more electrode pins between an IC package and a substrate from the outside in the above-mentioned composition, It prevents absorbing the external force added to a substrate and adding this external force to the root by the side of the IC package of a lead pin directly.

[0011]

JPO and INPIT are not responsible for any damages caused by the use of this translation.

- 1. This document has been translated by computer. So the translation may not reflect the original precisely.
- 2.\*\*\*\* shows the word which can not be translated.
- 3.In the drawings, any words are not translated.

### **EXAMPLE**

# [Example]

Hereafter, the example of this design is described with reference to drawings.

The mounting structure of the IC package whose <u>drawing 1</u> is one example of this design, and <u>drawing 2</u> show the sectional view cut with A-A' in <u>drawing 1</u>. In <u>drawing 1</u> and <u>drawing 2</u>, identical codes are given to <u>drawing 5</u> and identical parts, and detailed explanation is omitted. [0012]

In <u>drawing 1</u> and <u>drawing 2</u>, 2 is an insulating spacer. When this spacer 2 attaches IC package 1 to the substrate 3, it is beforehand attached to the substrate 3. And the radial lead pin 4 between IC package 1 and the substrate 3 exposes this spacer 2 so that clearly from <u>drawing 2</u>. [0013]

As for the spacer 2, the binder 6 is applied to the peripheral part. This binder 6 can be formed so that IC package 1 may float and an opening may not be made between the spacers 2, and adhesives may be sufficient as it.

[0014]

It is [ anything ] good if it is an existing elastic body of heat resistance, such as silicone rubber, as a material of the spacer 2. Furthermore, the spacer 2 is provided with uniform thickness and the hole 5 which a radial lead pin penetrates as shown in <u>drawing 3</u> is formed.
[0015]

This spacer 2 is not restricted to the above-mentioned composition. For example, the same operation as the spacer 2 which allotted the hole 5 for positioning to four corners, and showed drawing 1 and drawing 3 other partial foil \*\*\*\*\*\*\* as shown in drawing 4 is obtained. Although not illustrated, it cannot be overemphasized that the hole 5 is not formed but it may be made to pass a spacer only to a peripheral part.

[0016]

As stated above, since garbage etc. do not trespass upon the space between an IC package and a substrate according to this design, neither a malfunction nor bad insulation is woken up. The accident under attachment work can also be prevented. Generally, although a fin is attached to the upper surface in IC of PGA for heat dissipation of a chip, if the structure of this design is used, there will be few ventilation cross—section areas and they will end. That is, the effect of an air cooling with blower can be enlarged more by stopping the flow of the air of IC lower part. The spacer itself is an elastic body and the root of a radial lead pin does not become weak to the stress (external force) concerning a substrate.

[0017]

JPO and INPIT are not responsible for any damages caused by the use of this translation.

1. This document has been translated by computer. So the translation may not reflect the original precisely.

2.\*\*\*\* shows the word which can not be translated.

3.In the drawings, any words are not translated.

### **DESCRIPTION OF DRAWINGS**

[Brief Description of the Drawings]

[Drawing 1] The figure showing the composition of one example of this design.

[Drawing 2]The figure showing the section of drawing 1.

[Drawing 3]The perspective view showing an example of a spacer

[Drawing 4] The perspective view showing an example of a different spacer from drawing 3.

[Drawing 5]The sectional view showing the fitting structure of the conventional IC package.

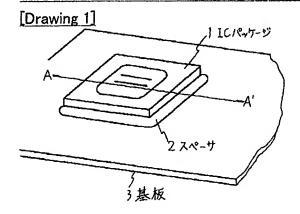
[Description of Notations]

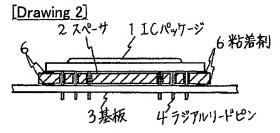
1 [ -- A radial lead pin, 5 / -- A hole, 6 / -- Binder ] -- An IC package, 2 -- A spacer, 3 -- A substrate, 4

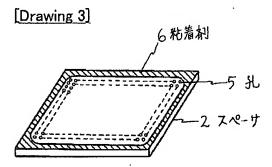
JPO and INPIT are not responsible for any damages caused by the use of this translation.

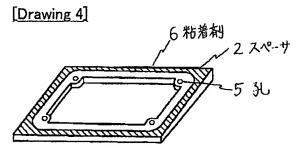
- 1. This document has been translated by computer. So the translation may not reflect the original precisely.
- 2.\*\*\* shows the word which can not be translated.
- 3.In the drawings, any words are not translated.

## **DRAWINGS**









[Drawing 5]

